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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LO, SUZANNE	

ART UNIT	PAPER NUMBER
2128	

NOTIFICATION DATE	DELIVERY MODE
10/22/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/675,748	NOURI ET AL.	
	Examiner	Art Unit	
	Suzanne Lo	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,11,15-19,21-25 and 28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,11,15-19,21-25 and 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-8,11,14-19,21-25 and 28 have been presented for examination.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 1-8 and 28 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Specifically, the claims are directed to software per se (configured simulators, comparator, and user data).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. **Claims 1-5, 7-8, 11, 14-16, 18-19, 21-25, and 28 are rejected** under 35 U.S.C. 103(a) as being unpatentable over **McNamara et al. (U.S. Patent No. 6,141,630) in view of Cavanaugh et al. (U.S. Patent No. 6,871,298 B1).**

As per claim 1, McNamara is directed to a system for evaluating a simulation design comprising: a reference simulator configured to execute a simulation image to obtain golden data, wherein the simulation image is a complied version of the simulation design **(column 5, lines 32-45)**; a test simulator **(column 3, lines 34-37 and Figure 1, testbench 108)** configured to execute the simulation image to obtain test data, wherein the test simulator is associated with a first implementation of the simulation design and the reference simulator is associated with a second implementation of the simulation design **(column 4, line 66 – column 5, line 4)**; and a comparator configured to generate a comparison result by comparing a portion of the golden data to a portion of the test data before the execution of the simulation image on the test simulator has completed **(column 7, lines 18-36)** wherein user data is used by the comparator to select the portion of the golden data and the portion of the test data **(column 4, lines 46-57 and column 5, 38-57)**; and wherein the comparison result is used to debug at least one selected from the group of the simulation design and the test simulator, by correcting and displaying an error detected in the comparison result **(column 7, lines 19-31)** but fails to explicitly disclose wherein the user data comprises a plurality of mapping rules used by the comparator to map *an internal hierarchy of* the first implementation of the simulation design to *an internal hierarchy of* the second implementation of the simulation design.

Cavanaugh teaches wherein the user data comprises a plurality of mapping rules used by the comparator to map *an internal hierarchy of* the first implementation of the simulation design to *an internal hierarchy of* the second implementation of the simulation design **(column 6, line 39 – column 7, line 13 and column 3, line 60 – column 4, line 22)**. It would have been obvious to an ordinary person skilled in the art at the time of the invention to combine the method of verifying a simulation design of McNamara with the user data of Cavanaugh in order to provide greater test coverage than static testing in a shorter amount of time **(column 2, lines 39-47)**.

As per claim 2, the combination of McNamara and Cavanaugh already discloses the system of claim 1 further comprising: a golden data repository storing the golden data **(column 5, lines 32-45)**; and a compiler configured to generate the simulation image by compiling the simulation design and user data **(column 7, lines 12-19)**.

As per claim 3, the combination of McNamara and Cavanaugh already discloses the system of claim 1, wherein comparing the portion of the golden data to the portion of the test data occurs dynamically **(column 7, lines 19-36)**.

As per claim 4, the combination of McNamara and Cavanaugh already discloses the system of claim 3 further comprising: a buffer to store the golden data **(column 5, lines 32-45)**.

As per claim 5, the combination of McNamara and Cavanaugh already discloses the system of claim 4, wherein the comparator is configured to wait to compare the portion of the test data until after the golden data is stored in the buffer **(column 5, lines 32-45)**.

As per claim 7, the combination of McNamara and Cavanaugh already discloses the system of claim 2, wherein user data is obtained before the test simulator has completed executing the simulation image **(column 4, lines 46-57)**.

As per claim 8, the combination of McNamara and Cavanaugh already discloses the system of claim 7, wherein user data is obtained while the test simulator is halted **(column 4, lines 46-57)**.

As per claim 11, McNamara is directed to a method of evaluating a simulation design comprising: executing a simulation image on a reference simulator to obtain golden data, wherein the simulation image is *obtained* by compiling the simulation design **(column 5, lines 32-45)**; executing the simulation image on a test simulator, wherein the test simulator is associated with a first implementation of the simulation design and the reference simulator is associated with a second implementation of the simulation design **(column 3, lines 34-37 and Figure 1, testbench 108)** to obtain test data **(column 4, line 66 – column 5, line 4)**; selecting a portion of the golden data and a portion of the test data **(column 4, lines 46-57 and column 5, 38-57)**; and comparing the selected portion of the golden data to the selected portion of the test data to obtain a comparison result **(column 7, lines 18-36)** wherein user data is used to select the portion of the golden data and the portion of the test data, and wherein the comparison result is used to debug at least one selected from the group of the simulation design and the test simulator, by correcting and displaying an error detected in the comparison result **(column 7, lines 19-31)** but fails to explicitly disclose wherein the user data comprises a plurality of mapping rules used by the comparator to map *an internal hierarchy of* the first implementation of the simulation design to *an internal hierarchy of* the second implementation of the simulation design.

Cavanaugh teaches wherein the user data comprises a plurality of mapping rules used by the comparator to map *an internal hierarchy of* the first implementation of the simulation design to *an internal hierarchy of* the second implementation of the simulation design **(column 6, line 39 – column 7, line 13 and column 3, line 60 – column 4, line 22)**. It would have been obvious to an ordinary person skilled in the art at the time of the invention to combine the method of verifying a simulation design of McNamara with the user data of Cavanaugh in order to provide greater test coverage than static testing in a shorter amount of time **(column 2, lines 39-47)**.

As per claim 15, the combination of McNamara and Cavanaugh already discloses the method of claim 11 further comprising: storing the golden data in a golden data repository **(column 5, lines 32-45)**.

As per claim 16, the combination of McNamara and Cavanaugh already discloses the method of claim 11, wherein the step of selecting a portion of the golden data is performed dynamically **(column 4, lines 46-57)**.

As per claim 18, the combination of McNamara and Cavanaugh already discloses the method of claim 11, wherein the step of comparing the selected golden data to the selected test data waits on storing the golden data in a buffer **(column 5, lines 32-45)**.

As per claim 19, the combination of McNamara and Cavanaugh already discloses the method of claim 11, wherein the step of selecting a portion of the test data is performed dynamically **(column 4, lines 46-57)**.

As per claim 21, the combination of McNamara and Cavanaugh already discloses the method of claim 20, wherein user data is obtained during the step of executing the simulation image on the test simulator **(column 7, lines 12-19)**.

As per claim 22, the combination of McNamara and Cavanaugh already discloses the method of claim 21, wherein the step of executing the simulation image is halted to obtain the user data **(column 4, lines 46-57)**.

As per claim 23, the combination of McNamara and Cavanaugh already discloses the method of claim 20, wherein user data comprises a mapping rule to map an implementation of the simulation design for the test simulator to an implementation of the simulation design for the reference simulator **(column 5, lines 46-54)**.

As per claim 24, the combination of McNamara and Cavanaugh already discloses the method of claim 11, wherein the step of comparing the selected golden data to the selected test data is performed before completing the step of executing the simulation image on the test simulator **(column 7, lines 18-36)**.

As per claim 25, McNamara is directed to a computer system for evaluating a simulation design comprising: a processor; a memory; a storage device; and software instructions **(column 6, lines 20-31)** stored in the memory for enabling the computer system to perform method steps with the same limitations as claim 11 and is therefore rejected over the same prior art combination.

As per claim 28, McNamara is directed to an apparatus **(column 6, lines 20-31)** for evaluating a simulation *design* comprising means for method steps with the same limitations as claims 11 and is therefore rejected over the same prior art combination.

4. **Claims 6 and 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over McNamara et al. (U.S. Patent No. 6,141,630) in view of Cavanaugh et al. (U.S. Patent No. 6,871,298 B1) **in further view of Davidson et al (U.S. Patent No. 6,886,145 B2).**

As per claim 6, the combination of McNamara and Cavanaugh is directed to the system of claim 5, but fails to disclose wherein the test simulator and the reference simulator execute the simulation image in lockstep.

Davidson teaches verification of partitioned testbenches in parallel **(column 8, lines 10-17)**. McNamara, Cavanaugh and Davidson are analogous art because they are from the same field of endeavor, verifying and validating circuit designs. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the system of verifying a circuit design of McNamara and Cavanaugh with the lockstep simulations of Davidson in order to shorten the verification time **(column 1, lines 46-51)**.

As per claim 17, the combination of McNamara and Cavanaugh is directed to the method of claim 16, but fails to disclose wherein the step of executing the simulation image on the test simulator and the step of executing the simulation image on the reference simulator is performed in lockstep. Davidson teaches verification of partitioned testbenches in parallel **(column 8, lines 10-17)**. McNamara,

Cavanaugh and Davidson are analogous art because they are from the same field of endeavor, verifying and validating circuit designs. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of verifying a circuit design of McNamara and Cavanaugh with the lockstep simulations of Davidson in order to shorten the verification time **(column 1, lines 46-51)**.

Response to Arguments

5. Applicant's arguments filed 08/01/07 have been fully considered but they are not persuasive.

6. The 35 U.S.C. 101 rejection is maintained for claims 1-8 and 28 are directed to software per se, all elements of the system of claims 1-8 and apparatus of claim 28 can consist solely of software – reference simulator, test simulator, comparator, test data with no accompanying medium. The 35 U.S.C. 101 rejection of claims 11, 15-19, 21-25 are withdrawn. However, the Applicant is advised that claim 25 while statutory, is directed to a computer system, with software instruction for enabling a computer system. As the instructions have limitations under intended use, the limitations following software instructions is not given patentable weight and claim 25 is anticipated by any computer system with processor, memory, and storage device.

7. The claim objection has been withdrawn due to the amended claims.

8. In response to Applicant's argument that Cavanaugh does not teach mapping rules for mapping an internal hierarchy of a first design to an internal hierarchy of a second design implementation only instruction grouping rules, the instruction grouping rules of Cavanaugh (column 8, lines 21-24) are part of a larger rule set which generates mapping rules mapping the golden data to the test data (column 3, lines 60 – column 4, line 22). As taught in column 4, of Cavanaugh, instructions will be eliminated that are ineligible for selection, one of the reasons being that the instructions conflict with the instruction grouping rules appropriate for the golden model and the processor system under test. The chosen instructions to run in parallel execution are then used for comparison and verification; column 5, lines 12-18 reads, "The present invention provides the processor developer with a test comprising a set of pseudo-

randomly generated instructions that include instruction packets appropriate for parallel execution, plus time-based intermediate state information produced when those instructions are executed on a golden model, that can then be run on the processor under test for comparison and verification." The same instructions are run between the golden simulator and the test simulator, and mapped to one another for comparison due to the rules of selecting instructions to run, and thus the internal hierarchy of one simulator is mapped to the internal (perhaps identical) hierarchy of another simulator.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. The prior art made of record is not relied upon because it is cumulative to the applied rejection. These references include:

1. U.S. Patent No. 6,678,645 B1 issued to Rajsuman et al. on 01/13/04.

2. U.S. Patent No. 6,625,759 B1 issued to Petsinger et al. on 09/23/03.

3. U.S. Patent No. 7,139,936 B2 issued to Petsinger et al. on 11/21/06.

4. U.S. Patent No. 6,606,721 B1 issued to Gowin, Jr. et al. on 08/12/03.

5. U.S. Patent No. 5,928,334 issued to Mandyam et al. on 07/27/99.

6. U.S. Patent No. 5,920,490 issued to Peters on 07/06/99.

7. U.S. Patent Application Publication 2005/0120278 A1 published by Smith et al. on 06/02/05.

10. All Claims are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suzanne Lo whose telephone number is (571)272-5876. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-2297. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Suzanne Lo
Patent Examiner
Art Unit 2128

SL
10/12/07

KAMINI SHAH
SUPERVISORY PATENT EXAMINER